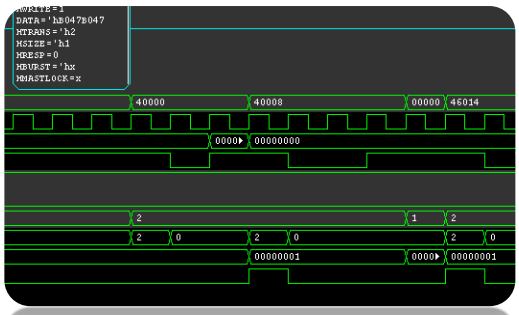
ANKASYS SVV-3D

ANKASYS TRAININGS



- Anka Microelectronic Systems offers verification trainings, which covers everything you need to get you started with advanced verification techniques.
- The ANKASYS SVV-3D is a SystemVerilog for Verification training, which covers the SystemVerilog language constructs that are specific to verification.
- The training introduces SystemVerilog Assertions as well, but for a comprehensive training, please take a look at ANKASYS SVA-3D , which is designed to cover all the aspect of assertion based verification.

Training Content

DAY 1

- Introduction to metric/coverage driven constrained random verification.
- Introduction to object oriented design methodology
- Introduction to verification components
- Static and dynamic domains of a testbench
- Introduction to new SystemVerilog data types

DAY 2

- Detailed analysis of new data types (dynamic arrays, queues etc.)
- Process synchronization (mailbox, semaphore, events etc.)
- Applying randomization at different levels of testbench
- Transaction level modeling (TLM)

DAY 3

- Covergroups and coveritems
- Assertion based verification and SystemVerilog assertions (SVA)
- Direct programming interface(DPI) and its differences compared to Verilog Procedural Interface (VPI)
- Introduction to Universal Verification Methodology (UVM)
- Verification planning and management (vPlan)

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