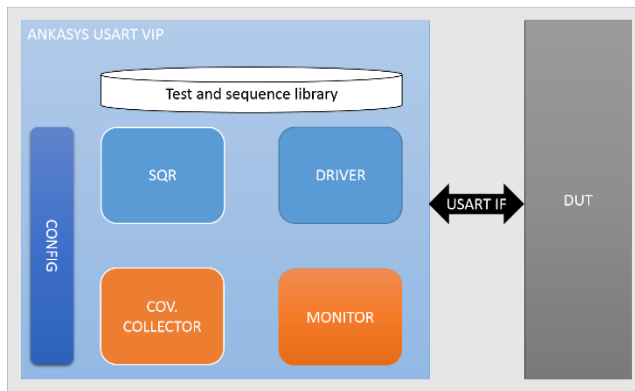


ANKASYS USART UVCS



- ➔ Anka Microelectronic Systems offers a unique USART verification package, where both the universal verification component and corresponding integration and training services are included in a single so called UVCS (Universal Verification Component and Services) package.
- ➔ Implementation is done in pure SystemVerilog language. No third party language or script is needed to integrate the IP.
- ➔ The complete component hierarchy inside the verification IP and corresponding test codes (sequences and tests) are all driven from UVM standard library. No customized vendor specific code.

Key IP Features

- Easy integration and user interface.
- Ready-to-use default USART configuration with a pre-defined baud rate.
- Dynamic baud rate adjustment.
- Automatic clock frequency calculation.
- Adjustable min and max character lengths
- Parametric parity check
- Selectable MSB or LSB first options
- Random and selectable pre/post delay injections.
- Pre-defined Systemverilog covergroups for coverage collection.
- Pre-defined USART sequences.
- An example UVM testbench with a simplified DUT

Available Services

- Integration Support
- Application Support
- Customization
- Maintenance



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